IDEC Chip Design Contest

A 16.3 dBm 14.1 % PAE 28-dB Gain W-band Push-Pull Power Amplifier Utilizing Inductive Feedback in 65-nm CMOS

dongguk UNIVERSITY

Van-Son Trinh and Jung-Dong Park

Division of Electronics and Electrical Engineering, Dongguk University

Introduction

- A push-pull structure using a differential pair of transistors has been widely used to improve output power in designing power amplifier (PA).
- To stabilize the differential pair of the active device, a common technique is using capacitive cross-coupled neutralization.
- However, the required cross-coupled capacitor for a W-band PA is typically in the range of several femto-farads, which is difficult to rely on in practice. Moreover, this suffers from low quality factor of the cross-coupled capacitor, which degrades the performance of the PA.
- In this paper, we present an 82 GHz push-pull PA with inductive uni-laterization to achieve a well-balanced overall PA performance.

PA Design

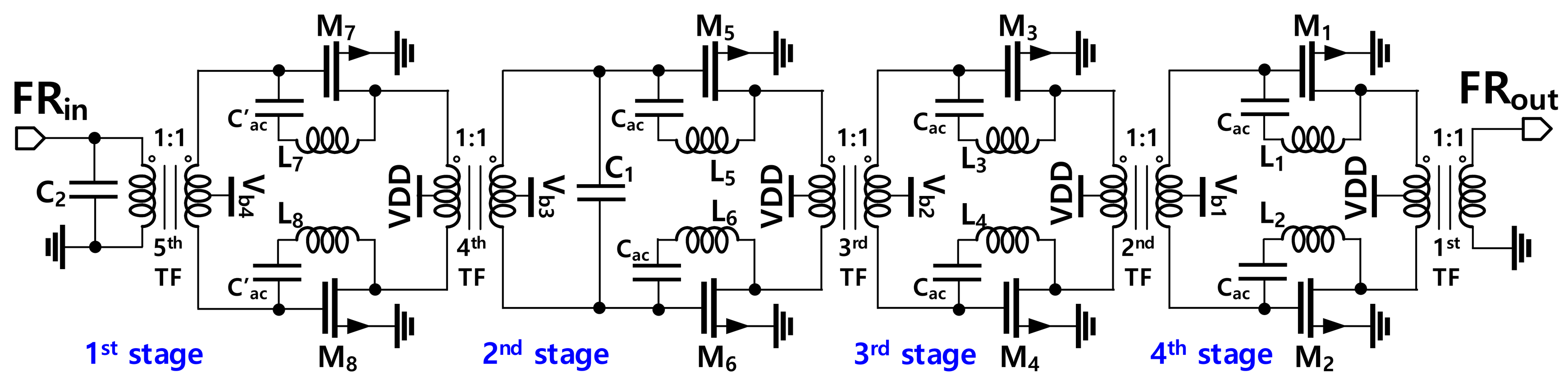
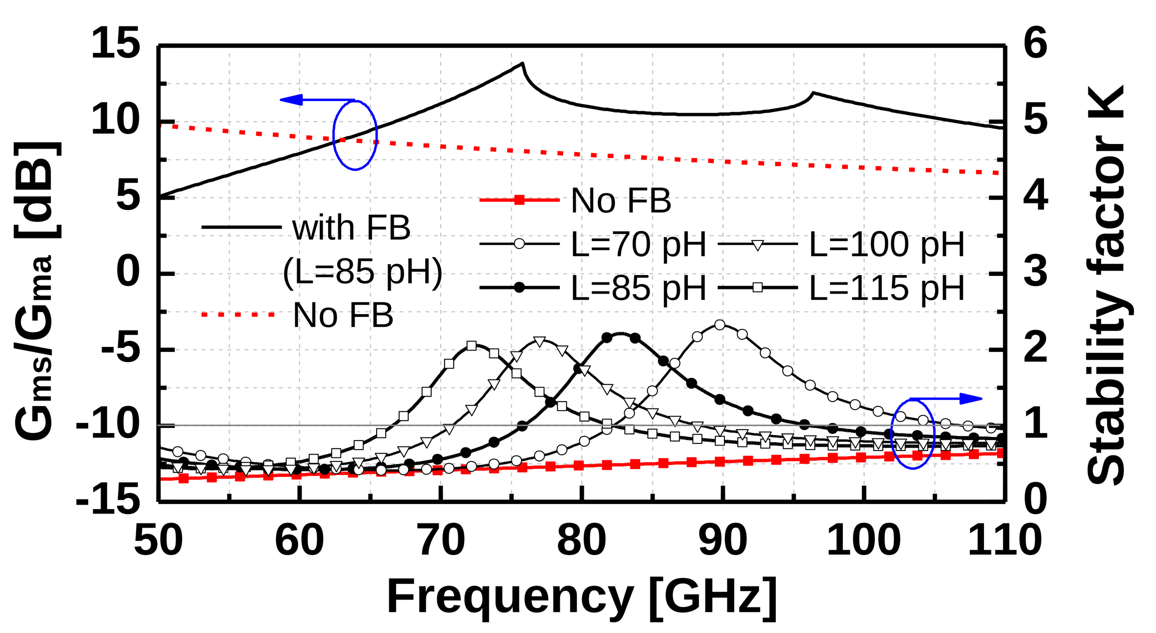


Fig. 1. Schematic of the propose inductive feedback push-pull power amplifier.



M_1-M_2: 176u L_1-L_2: 85 pH
M_3-M_4: 112u L_3-L_8: 153 pH
M_5-M_8: 88u Q_1-Q_2: 17.2
C_1: 20.4 fF Q_3-Q_8: 15.9
C_2: 22.2 fF C_{ac}: 267 fF
C_{ac}: MIM cap C'_{ac}: 208 fF
C'_{ac}: MIM cap and moscap
V_{b1}-V_{b4}: 0.7 V

Fig. 2. Design feedback inductor of the fourth stage of the PA: Gms/Gma and stability factor K versus frequency of several cases of feedback (FB) inductor.

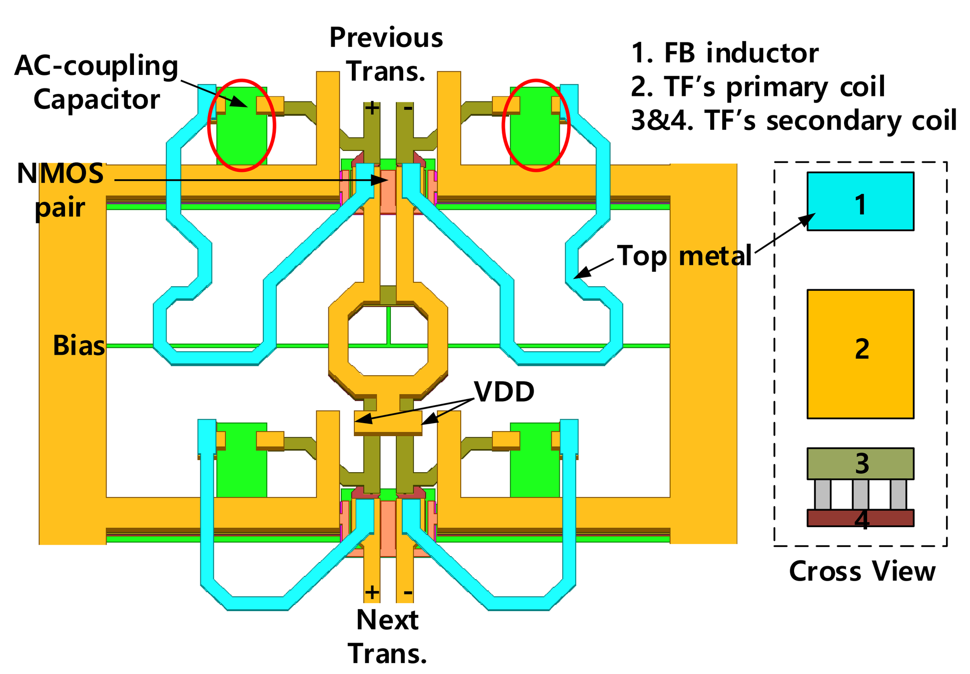


Fig. 3. Physical layout of a push-pull amplifier stage with an inductor feedback.

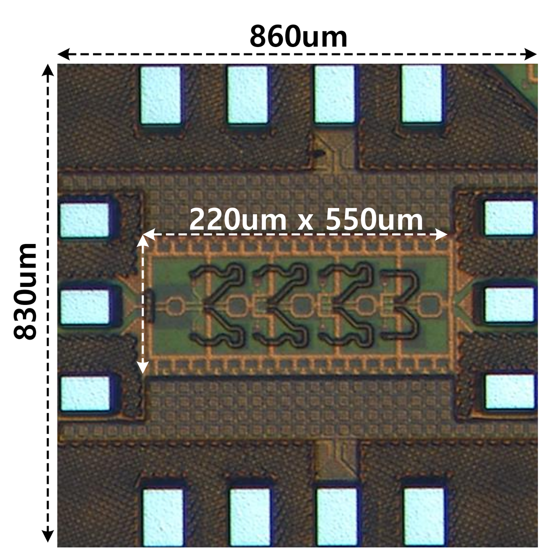


Fig. 4. Chip photograph of the fabricated PA.

Measurement results

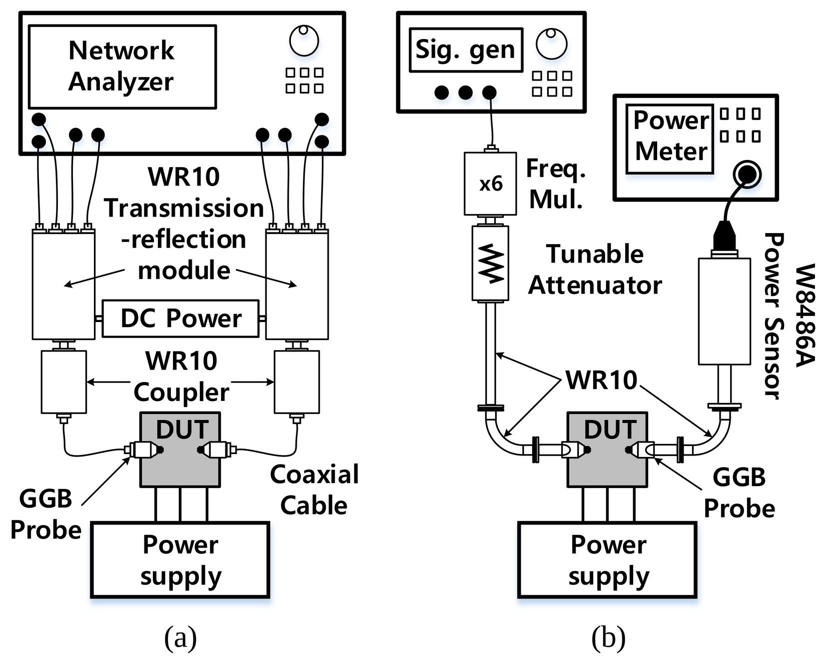


Fig. 5. Measurement setup for (a) S-parameters and (b) Large-signal performances.

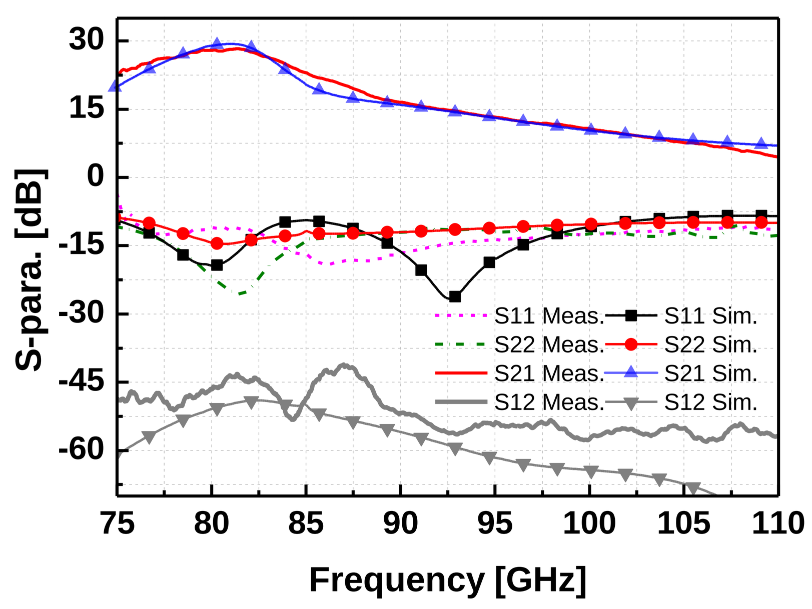


Fig. 6. Simulated and measured S-parameters of the PA.

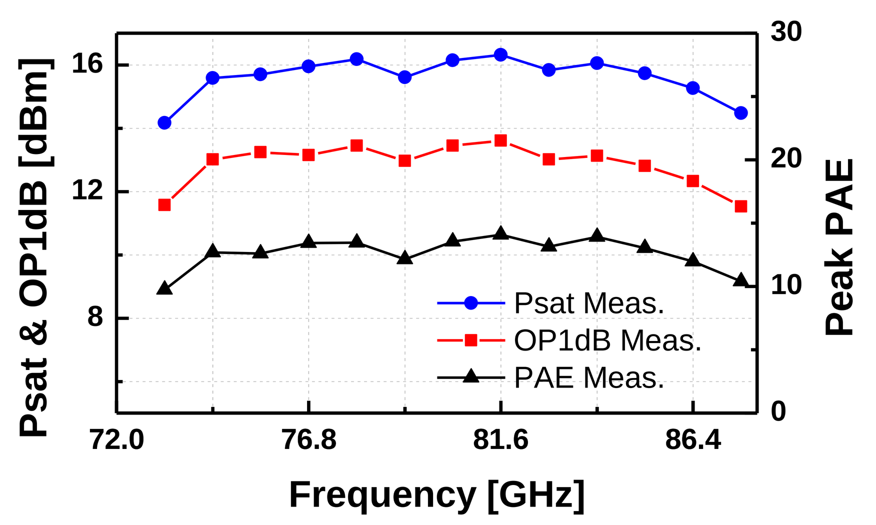


Fig. 7. The measured saturated output power (Psat), output 1-dB gain compression point (OP1dB) and power added efficiency (PAE) of the PA.

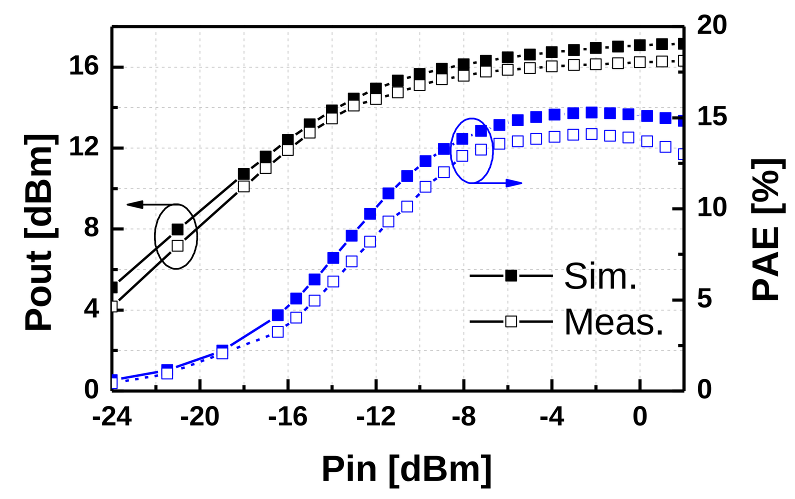


Fig. 8. The measured and simulated output power (Pout) and PAE versus input power (Pin).

Comparison table

Ref.	Tech. (CMOS)	Topology	Freq. (GHz)	VDD (V)	P_{sat} (dBm)	Gain (dB)	Peak PAE (%)	OP1dB (dBm)	Area (mm^2)	DC-Diss. [mW]	FOM
[1]	65-nm	4-way com.	100-117@109	1.2	15.2	20.3	10.3	12.5	0.34	NA	86.4
[2]	65-nm	16-way com.	77-103@90	1.2	18.3	12.5	9.5	17.5	0.82	NA	79.7
[3]	65-nm	4-way com.	84.0-88.8@87	1	11.9	18.6	9.0	9.6	0.37	NA	78.8
[4]	90-nm	4-way com.	86-98@94	2.4	16.8	20	16.4	15	0.69	280	88.4
[5]	65-nm	4-way com.	77	2	15.8	20.9	15.2	13	0.21*	246	86.2
[6]	90-nm	2-way com.	69-81@76	2.4	12.8	21.5	9.9	9.5	0.36	182.4	81.9
[7]	40-nm	4-way com.	70.3-85.5@80	0.9	20.9	18.1	22.3	17.8	0.19*	375	90.5
[8]	65-nm	2-way com.	68-78@75	1.3	17.3	21.4	18.9	14.6	0.09*	284.7	89.0
[9]	45-nm SOI	Multi-drive 3-stack	91	3.4	19.2	12.4	14	NA	0.228*	379	82.2
[10]	65-nm	2-way com.	57.2-66.9@~62	1.2	14.35	20.9	21.1	11.68	0.088*	126	84.3
This	**65-nm**	**2-way com.**	**76.8-83.8@81.6**	**1.2**	**16.3**	**28.3**	**14.1**	**13.6**	**0.72 (0.121*)**	**234**	**94.3**

*PA core only; $FOM = P_{sat}(\text{dBm}) + Gain(\text{dB}) + 10\log\left(PAE[\%] \times f^2[\text{GHz}]\right)$

1. H. S. Son, J. Y. Jang, D. M. Kang, H. J. Lee, and C. S. Park, "A 109 GHz CMOS Power Amplifier With 15.2 dBm Psat and 20.3 dB Gain in 65-nm CMOS Technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 7, pp. 510–512, Jul. 2016.
2. Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao, and H. Wang, "Millimeter-wave CMOS power amplifiers with high output power and wideband performances," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4520–4533, Dec. 2013.
3. H. Jia, B. Chi, L. Kuang, and Z. Wang, "A W-band Power Amplifier Utilizing a Miniaturized Marchand Balun Combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 719–825, Feb. 2015.
4. Y.-S. Lin, and V. K. Nguyen, "94-GHz CMOS Power Amplifiers Using Miniature Dual Y-Shaped Combiner with RL Load," *IEEE Trans. Circ. and Syst.–I: Reg. Papers*, vol. 64, no. 6, Jun. 2017.
5. J. Oh, B. Ku, and S. Hong, "A 77-GHz CMOS Power Amplifier with a Parallel Power Combiner Based on Transmission-Line Transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2662–2669, Jul. 2013.
6. J.-H. Tsai, R.-A. Chang, and J.-Y. Lin, "A 69–81 GHz power amplifier using 90nm CMOS technology," in *Proc. IEEE 14th Topical Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Jan. 2014, pp. 77–79.
7. D. Zhao and P. Reynaert, "A 0.9V 20.9dBm 22.3%-PAE E-band power amplifier with broadband parallel-series power combiner in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 248–249.
8. T. Xi, S. Huang, S. Guo, P. Gui, D. Huang, and S. Chakraborty, "High-efficient E-band power amplifiers and transmitter using gate capacitance linearization in 65 nm CMOS process," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 64, no. 3, pp. 234-238, Mar. 2017.
9. A. Agah, J. A. Jayamon, P. M. Asbeck, L. E. Larson, and J. F. Buckwalter, "Multi-drive stacked-FET power amplifiers at 90 GHz in 45 nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1148–1157, May 2014.
10. W.X. Ye, K. Ma, K. S. Yeo, and Q. Zou., "A 65 nm CMOS Power Amplifier with Peak PAE above 18.9% From 57 to 66 GHz Using Synthesized Transformer-Based Matching Network," *IEEE Trans. Circ. and Syst.–I: Reg. Papers*, vol.62, no.10, pp.2533-2543, Oct. 2015.

Acknowledgements

This work was supported in part by the National Research Foundation of Korea grant funded by the Korea Government (MSIP) under Grant 2019M3F6A1106118, and in part by the IC Design Education Center for the chip fabrication and EDA tool.

반도체설계교육센터
IC DESIGN EDUCATION CENTER